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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,577	10/07/2003	Christopher J. Diorio	IMPJ-0004 033327-000036	6797

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EXAMINER	
NGUYEN, HAI L	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,577	DIORIO ET AL.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 1974*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 27-51* is/are pending in the application.

4a) Of the above claim(s) *18-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,27-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/13/04 & 9/7/04* 6/7/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-17 and 27-51, drawn to a signal processing circuit with parallel controlled paths having an embodiment as shown in Figs. 5A-5B, classified in class 327, subclass 403.

   II. Claims 18-26, drawn to a delay controlled circuit having an embodiment as shown in Fig. 4A, classified in class 327, subclass 392.

2. Inventions group I, group II, group III and group IV are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination (group I) as claimed does not require the particulars of the subcombination as claimed (group II). The recited combination of the signal processing circuit comprises the delay controlled circuit may, by itself, be pantentable over prior art. The subcombination of group II has separate utility, i.e., the delay controlled circuit can be used in many different types of circuits such as, for example, a ring oscillator circuit.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Mr. David Ritchie on 12/06/04 a provisional election was made without traverse to prosecute the invention of group I, claims 1-17 and 27-51. Affirmation of this election must be made by applicant in replying to this Office action. Claims 18-26 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(I).

Drawings

6. Figures 3A - 3D should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

7. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the recited limitations "an amount of charge present on the floating gate of the floating-gate transistor is used to match a first circuit characteristic in the first circuit pathway to a second circuit characteristic in a second circuit pathway of the circuit", in claim 33, and "means for modifying a first circuit characteristic in the first circuit path relative to a second circuit characteristic in the second circuit path by adjusting an amount of charge stored on a floating of the floating-gate field effect transistor", in claim 45, are **not supported** either by the disclosure or the drawings. There are insufficient antecedent basis for these limitations in the claims.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 12, the limitation "a first analog-valued floating-gate transistor", in line 11, lacks clear antecedent basis. It is unclear if this analog-valued floating-gate transistor is the same as the analog-valued floating-gate transistor recited in line 7 (or a different analog-valued floating-gate transistor). From the specification and drawings, it appears that "a second

analog-valued floating-gate transistor", in line 11, should be changed to --a first analog-valued floating-gate transistor--.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-17 and 27-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA), Figs. 1-2 in the present application, in view of Kliza et al. (US 5,852,640).

With regard to claim 1, the APA discloses in Figs. 1-2 an apparatus, comprising a time-interleaved system operable to distribute a signal into a first processing pathway and, following a predetermined amount of time, into a second processing pathway. The reference circuit meets all the claimed limitations except for a delay structure (96-1 – 96-m in instant Fig. 5B) coupled to the second processing pathway, the delay structure including at least one floating-gate field effect transistor. Kliza et al. teaches in Fig. 13 a similar time-interleaved system (109) having a delay structure (91 -94) as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize the delay structure taught by Kliza et al. al. with the reference circuit for the advantage of providing a self adjustable delay to maintain predetermined phase shift of multi-phase shifted clocks.

With regard to claims 2-3, the above discussed circuit of the references meets all of the claimed limitations except for the limitation that the intended use of the signal processing apparatus as an analog-to-digital converter or a quadrature mixing circuit. Kliza et al. teaches the delay structure for providing a self adjustable delay to maintain predetermined phase shift of multi-phase shifted clocks in a time-interleaved system. Since the analog-to-digital converter and the quadrature mixing circuit are also the time-interleaved system. Therefore, it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention was made to employ the analog-to-digital converter/the quadrature mixing circuit in the time-interleaved system of the reference for the benefit of self adjustable delay.

If Applicant does not agree that is an obvious reason, but rather it is a novel feature of the invention then this application will be entitled to consideration of further restriction. Since, there would be many patentably distinct species of the claimed invention in this application.

With regard to claim 4, the APA discloses in Figs. 1-2 a signal processing apparatus comprising an input node configured to receive a signal (CLOCK); a splitter (14) operable to split the signal into a first signal portion and a second signal portion and direct the first signal portion to a first node (16-1) and directing the second signal portion to a second node (16-M); and a first circuit (a switch controlled by signal Φ1 & 12-1) coupled between the first node and a third node (at the controlled node of the switch controlled by signal Φ1). The reference circuit meets all the claimed limitations except for a first circuit (96-1 – 96-m in instant Fig. 5B) coupled between the first node and a third node. Kliza et al. teaches in Fig. 13 a similar signal processing apparatus (109) having first circuits (91 -94) including a first analog-valued floating-gate transistor operable to effect a time delay on the first signal portion depending on an

amount of electrical charge stored on a floating gate of the first transistor, as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize the circuits taught by Kliza et al. al. with the reference circuit for the advantage of providing a self adjustable delay to maintain predetermined phase shift of multi-phase shifted clocks.

With regard to claim 5, the signal processing apparatus further comprises a second circuit (a switch controlled by signal ΦM & 16-M) coupled between the second node and a fourth node.

With regard to claim 6, the signal processing apparatus further comprises a combiner (18) operable to combine signals from outputs of the first and second circuits.

Claim 7 is similarly rejected; note the above discussion with regard to claim 4.

Claims 8-17, 27-31 are similarly rejected; note the above discussion with regard to claims 4-7.

Claims 32-34 are similarly rejected; note the above discussion with regard to claims 1-3.

Claims 45 and 46 are similarly rejected; note the above discussion with regard to claims 4-7.

With regard to claims 35, 36, 47, and 48, since the claimed structure is met by the reference, inherently, the result functions of these claims will also be met.

With regard to claims 37 and 49, the circuit comprises a pipelined circuit (20).

Claims 38-43 and 50 are similarly rejected; note the above discussion with regard to claims 2-3.

With regard to claims 44 and 51, the reference also meets the recited limitation in this claim.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Tsujino (US Pat. 6,653,877) is cited as of interest because it discloses a semiconductor device capable of internally adjusting delayed amount of a clock signal.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
December 6, 2004

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